



DWC1225NS ESD Protection Diode

Feature

- Bi-directional ESD protection of one line
- 48Watts peak pulse power ($t_p=8/20\mu s$)
- Working voltage: 3.3V
- Junction Capacitance: 0.4pF(Typ)
- Low leakage current
- Low clamping voltage
- IEC 61000-4-2 $\pm 12kV$ contact $\pm 15kV$ air
- IEC 61000-4-5 (Lightning) 6A (8/20 μs)
- IEC61000-4-4(EFT) 40A (5/50ns)

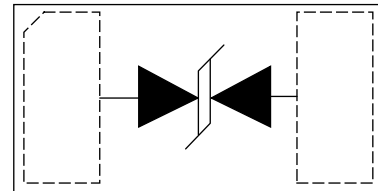
Application

- USB2.0/USB3.0
- HDMI1.3,HDMI1.4 and HDMI2.0
- SATA and eSATA interface
- Computers and peripherals
- Display and Cameras

Mechanical Data

- Package: DFN0603-2L
- Molding compound flammability rating: UL 94V-0
- RoHS/WEEE Compliant

Schematic & PIN Configuration



Ordering Information

Part Number	Package	Marking	Packing	Reel Size
DWC1225NS	DFN0603-2L		10000 Tape & Reel	7 inches

Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Maximum Peak Pulse Current ($t_p=8/20\mu\text{s}$)	I_{pp}	6	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	± 15 ± 12	kV
Lead Soldering Temperature	T_L	260(10sec.)	$^{\circ}\text{C}$
Junction Temperature	T_J	-55 to + 125	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55 to + 150	$^{\circ}\text{C}$

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reverse Stand-Off Voltage	V_{RWM}		-3.3		3.3	V
Reverse Leakage Current	I_R	$V_{RWM}=\pm 3.3\text{V}$			0.5	μA
Reverse Breakdown Voltage	V_{BR}	$I_T=1\text{mA}$	8			V
Reverse Holding Voltage	V_H	$I_T=I_H$		2.7		V
ESD Clamping Voltage ⁽¹⁾	V_C	$I_{TLP}=4\text{A}, t_p=0.2/100\text{ns}$		4.7		V
ESD Dynamic Resistance ⁽²⁾	R_{DYN}	$T_{LP}=0.2/100\text{ns}$		0.34		Ω
Clamping Voltage	V_C	$I_{PP}=6\text{A}, t_p=8/20\mu\text{s}$			8	V
Junction Capacitance	C_j	$V_R = 0\text{V}, f = 1\text{MHz}$		0.4	0.55	pF

Electrical Parameters

V_{RWM} Reverse Working Voltage Max.

I_R Maximum Reverse Leakage Current @ V_{RWM}

V_T Trigger Voltage

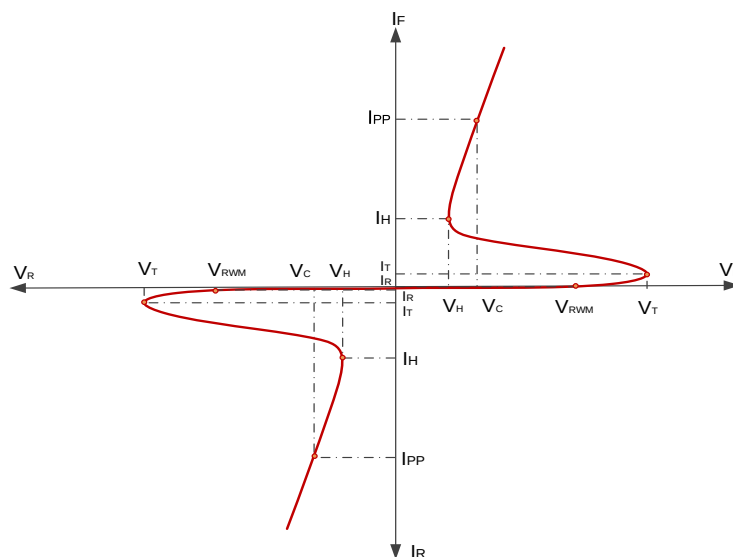
V_H Holding Voltage

I_H Holding Current

V_{BR} Reverse Breakdown Voltage

I_{PP} Maximum Reverse Peak Pulse Current

V_C Clamping Voltage @ I_{PP}



Note(1): TLP Setting: I_{TLP} and V_{TLP} sample window: $t_1=70\text{ns}$ to $t_2=90\text{ns}$.

Note(2): Dynamic resistance calculated from $I_{PP}=4\text{A}$ to $I_{PP}=16\text{A}$



Typical Characteristics

Figure1: 8/20 μ s pulse waveform according to IEC61000-4-5

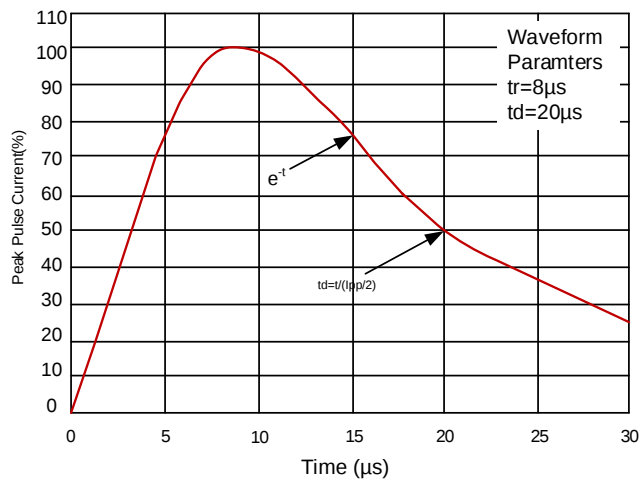


Figure2: ESD pulse waveform according to IEC 61000-4-2

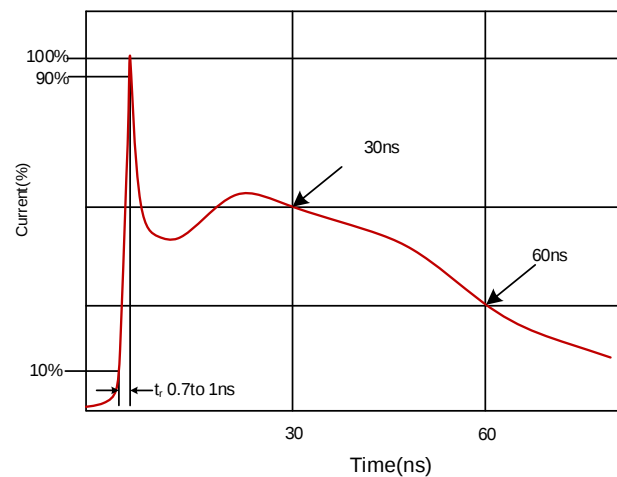


Figure3: Power Derating Curve

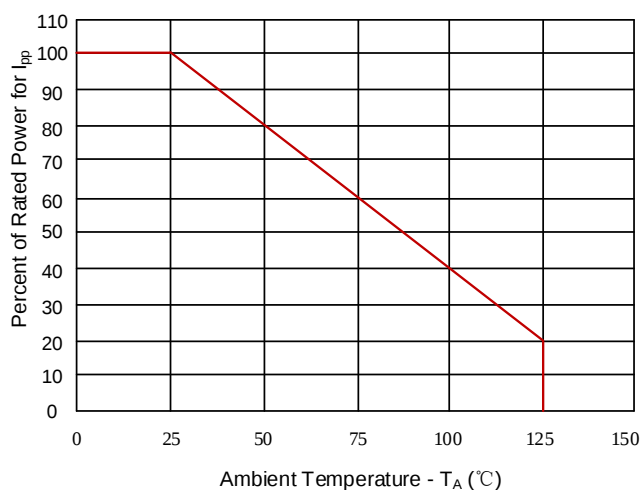


Figure 4: Clamping Voltage vs. I_{pp}

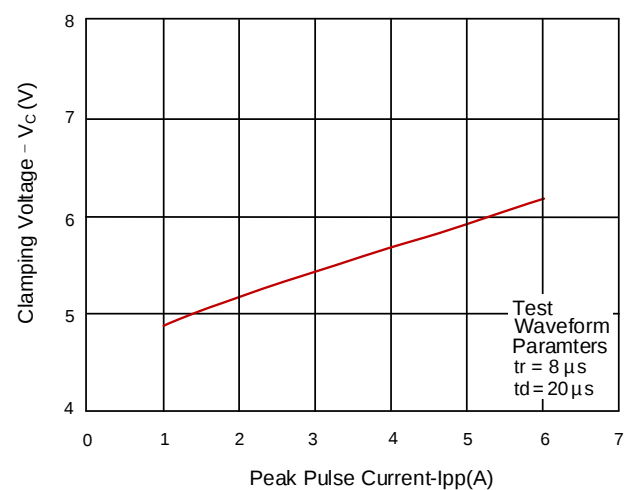


Figure5: TLP Positive I-V Curve

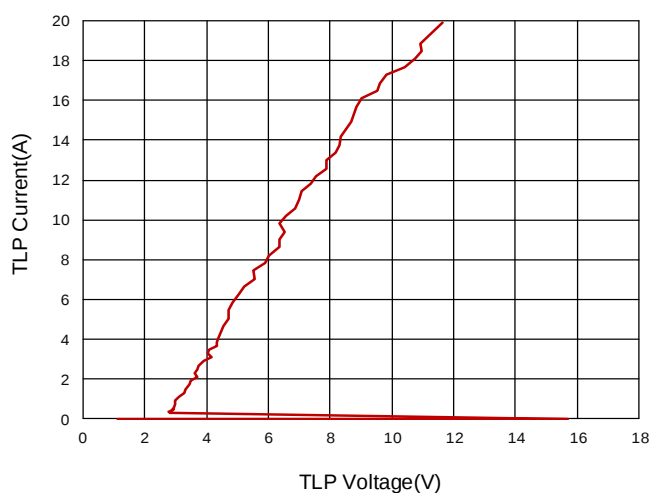
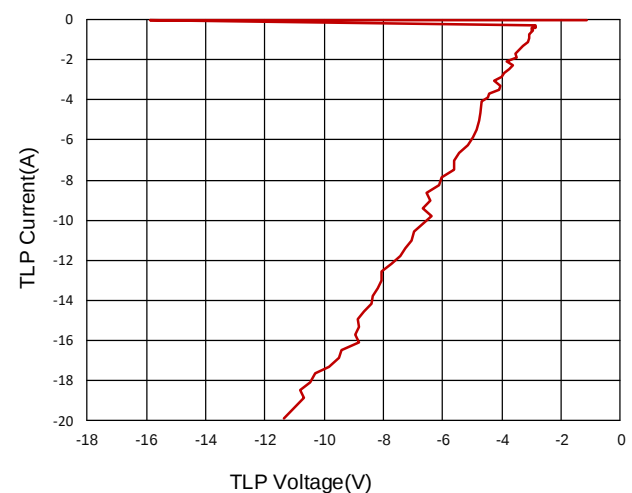
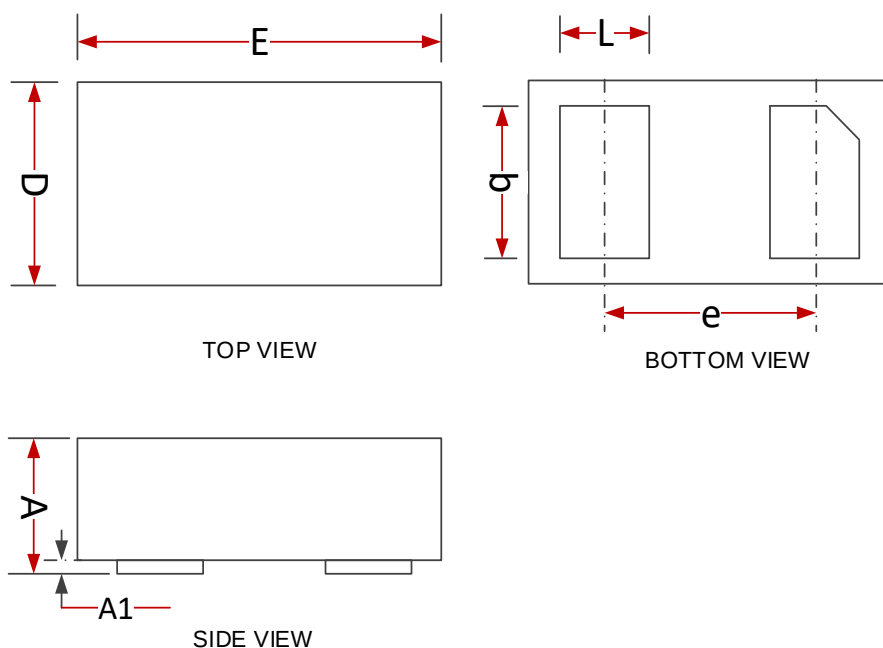


Figure6: TLP Negative I-V Curve



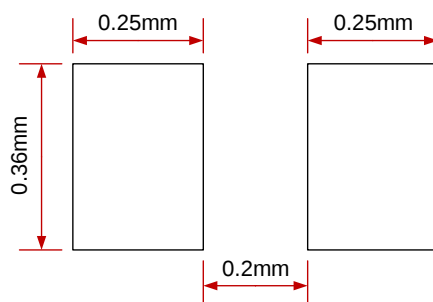


DFN0603-2L Outline Drawing



Common Dimension (mm)			
PKG	DFN0603-2L		
REF.	MIN.	NOM.	MAX.
A	0.28	0.30	0.34
A1	0.00	0.02	0.05
b	0.21	0.23	0.265
L	0.14		0.24
e	0.40BSC		
D	0.25	0.30	0.35
E	0.55	0.60	0.65

Land Pattern *



* This land pattern is for reference purposes only